Contents

1 MINERνA Electronics: Introduction

The requirements for the MINERνA electronics are summarized in Table 1. These requirements are motivated by the experiment's physics goals, which include:

- Fine-grained spatial resolution, exploiting light-sharing between neighboring scintillator strips,
- Identification of $\pi^{\pm}$, $K^{\pm}$ and p using dE/dx information,
- Efficient pattern-recognition, using timing to identify track direction and separate interactions occuring during a single spill,
- Ability to identify strange particles, and muon decay, using delayed coincidence, and
- Negligible deadtime within a spill.

The average data rate expected for MINERνA ($\sim$ 100 kByte/second) and the relatively modest duty-factor of the NuMI beam (one $\sim$ 10 μs spill every 2 seconds) are far from demanding, by the standards of modern high-energy physics experiments.

2 Front-end Electronics

The front-end boards digitize timing and pulse-height signals and provide high-voltage for the photo-multiplier tubes (PMTs), and communicate with VME-resident readout controller modules over an LVDS token-ring. For easy access in connection, testing and replacement, the boards are mounted *outside* the light-tight PMT housing assemblies. Pulse-heights and latched times will be read from all channels at the end of each spill.

The front-end board for MINERνA is designed around the D0 TriP-t ASIC which is a redesign of the readout ASIC for the D0 fiber tracker and preshower. The TriP-t chip has suitable capabilities for use in MINERνA. The most significant technical risks have already been addressed by our successful 2004 R&D program, using a prototype board fabricated using available TriP chips from D0.

2.1 Requirements and design features

Each front-end board (FEB) will service one PMT (64 channels) which will require 6 TriP-t chips per board. The TriP-t chips will be controlled by a commercial FPGA (Field-Programmable Gate Array) using custom firmware. A prototype of

this firmware has already been developed and successfully operated during our R&D studies. In addition to digitization of charge and timing information, the front-end boards will also supply high-voltage to the associated PMT and communicate with the downstream readout system over an LVDS (Low-Voltage Differential Signaling) link. The FEB will attach to the PMT box via the transition board that is mounted to the rear of the PMT box as shown in figure **??**. Figure 1 shows the basic design of the board and the main components. Table 2 summarizes the channel counts for the final design.

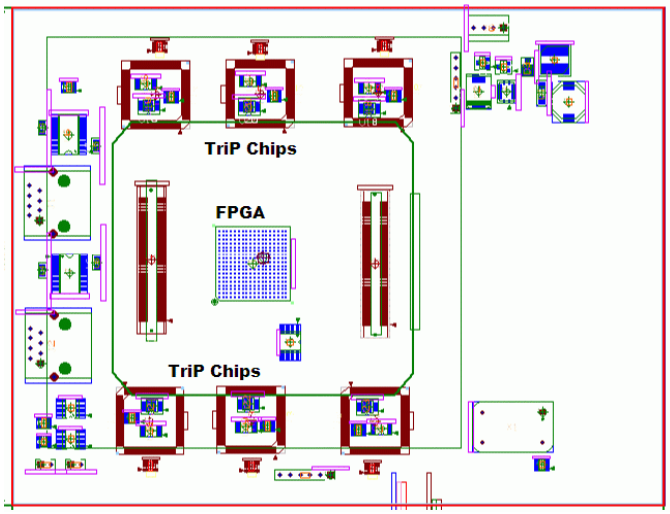

Figure 1: Simplified schematic of the front end electronics 2nd prototype board.

2.2 The TriP-t chip and digitization

The heart of the system is the D0 TriP-t ASIC. The TriP-t chip was designed by Abder Mekkaoui of the Fermilab ASIC group and has undergone extensive testing by D0 [1]. Its analog readout is based on the SVX4 chip design. Each TriP-t chip supports 32 channels for digitization, but only half that number of channels for discrimination and timing. A simplified schematic of the TriP-t ASIC is shown in Figure 2. The pre-amplifier gain is controlled by jumper GAIN(3) and has two settings which differ by a factor of four. The gain of the second amplifier stage is controlled by jumpers GAIN(2)-GAIN(0). We will set the chip to the highest gain setting for the preamp and lowest integration capacitor. This gives a linear range with a maximum charge readout of 1 pC. The "A OUTPUT" goes into a analog pipeline, which is identical to the one used on the SVX4 chip and 48 cells deep. To gain dynamic range, MINERνA will increase the input range of the electronics by using a passive divider to divide charge from a single PMT anode among three

Parameter	Value	Comments
Active spill width	12 μsec	Spill plus $2\tau_\mu$
Repetition Time	$>$ 1.9 sec	
Number of channels	30272	
Occupancy per spill	2%	LE beam, 2.5E13 POT/spill
Front-end noise RMS	$<$ 0.2 PE	
Photodetector gain variation	4.5 dB	Extremes of pixel-to-pixel variation
Minimum saturation	350 PE	Proton range-out or DIS event
Maximum guaranteed charge/PE	50 fC	Lowest possible charge at highest gain
Time resolution	3 ns	Identify backwards tracks by TOF
		Identify decay-at-rest $K^\pm$

Table 1: Electronics design requirements and parameters for MINERνA

Item	
Number of FEB boards including spares(15%))	545
Number of PMT's serviced per board	1
Number of PMT channels serviced per board	64
Number of ADC channels per board	192 (Low, Middle, High Gain)
Number of TDC channels per board	64
Number of HV channels per board	1

Table 2: MINERνA front-end board channel summary.

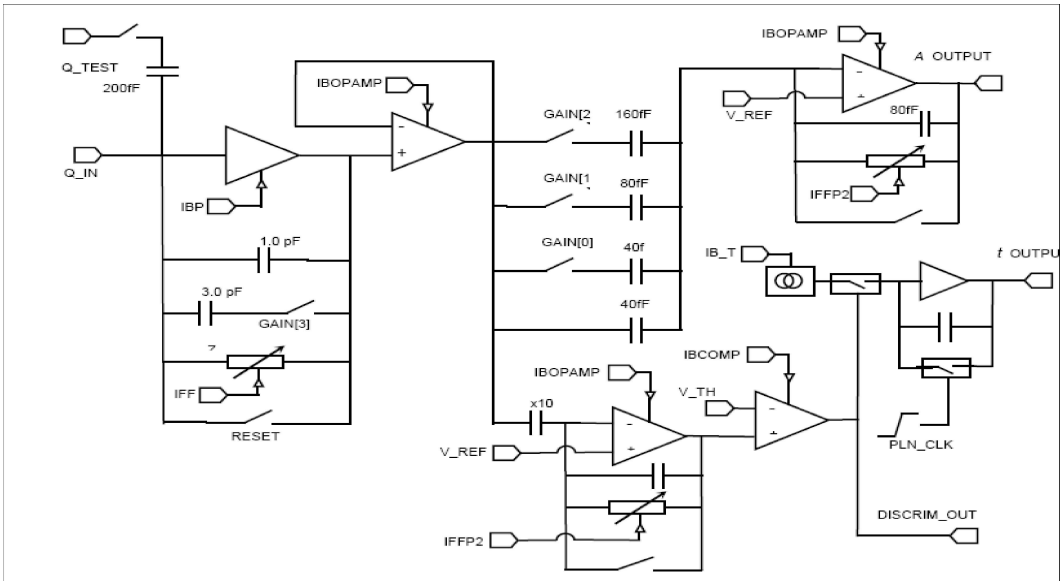

Figure 2: Simplified schematic of the front end electronics of the TriP-t chip.

TriP-t channels. Each TriP-t channel will be digitized by a 10 bit ADC.

Based on Monte Carlo studies of proton identification by dE/dx, the MINERνA design requires no saturation below 350 photoelectrons (PE) and RMS noise well below 1 PE. Matching this to the 1 pC charge limit, the highest gain anodes in a tube would be set at 100 fC/PE and therefore the lowest gain anodes would be run at 33 fC/PE. In MINERνA the integration time for the ADC will be 10–12 μs, much less than the hold time for the charge in the capacitor of 100 μs. The prototype MINERνA board has been tested explicitly with a 10 μs gate, and pedestal RMS was found to be $<$2 fC. This will put a single photoelectron approximately a factor of 10 above the pedestal RMS, well within our requirements. The maximum PMT gain for the lowest gain anode will be 50 fC/PE, safely within the desired parameters above.

2.3 Timing

Only one of every two input channels to the TriP-t chip have a latched discriminator output (latch) which can be used for timing information. Hence, only the lower range channels will feed the latch whose output will then go into an FPGA. With appropriate firmware, internal logic of the FPGA can be used measure timing with a granularity of 5 ns. To measure the time of the latch firing accurately, the RF/2 reference clock from the Tevatron (approximately 25Mhz) is multiplied by four in a PLL and phase shifted by 90deg to form a quadrature clock that is

used inside the FPGA to form a digital TDC with least bit resolution of 2.5ns. This feature has also been tested on the prototype board and a timing resolution consistent with the 2.5 ns least count timing resolution of the TDC's has been achieved. The reset time for the latch is only 15 ns, so inside a spill the latch will be in the ready state by default. When the signal exceeds a threshold of 1.5 PE, the latch will fire. After storing the time, the latch is reset, incurring minimal deadtime.

Each board includes its own high-frequency phase-locked oscillator, which provides a local clock signal for the FPGA logic. Global synchronization is provided using an external counter-reset reference signal distributed over the LVDS interface from the VME readout boards once every second, and originating with a MINOS timing module which is, in turn, synchronized to the NuMI beam.

2.4 High-voltage

A Cockroft-Walton(CW) high-voltage base supply will provide power to each board's PMT. The Cockroft-Walton high-voltage supply will be split between two boards: one that resides in the PMT box and contains passive components and a second board (Front-End Support Board - FESB) that will be attached to the outside of the PMT box. The CW card that resides in the PMT Box will also map the analog PMT pixel signals to connectors on the transition board. See figure **??** for details. The auxiliary card (FESB) design will allow a malfunctioning high-voltage supply to be easily replaced without changing the main readout board. An existing Cockroft-Walton controller design (developed at Fermilab) will allow the PMT voltage to be monitored, adjusted or disabled over computer control, using the LVDS interface.

2.5 LVDS interface

As detailed in Section 3 each front-end board will be a member of a chain (or token-ring) connected by LVDS to a VME-resident readout controller. As such, the front-end boards require two LVDS connections, one to receive data from the previous member, and another to transmit data to the next. The LVDS interface transmits all information to and from the board, including:

- Transmission of digitized timing and charge data from the front-end board to the VME readout controller,
- Write access to the front-end memory buffers, for diagnostics,
- Configuration of the TriP-t chip registers (thresholds, gains, etc) for data-taking,

- Reprogramming of the flash ROM containing the front-end board's FPGA firmware, and
- High-voltage control and monitoring messages.

The first prototype front-end board used in our 2004 R&D studies was designed to accommodate an LVDS interface, was commissioned and tested in late-2004/early-2005.[1] This subsystem represented the most significant remaining technical risk in the electronics (now that the TriP-t digitization and timing scheme has been successfully tested), as the latency in propagating signals from one front-end board to another via LVDS limits the number of boards that may be linked in a single chain, and hence the number of chains (and VME readout boards) required to service the full detector. The latency tolerance is constrained by the need to transmit a global timing synchronization signal to all front-end readout boards. As explained in Section 3, pending prototype testing we estimate approximately 100 ps jitter may be introduced by each link in the chain. As the least count of our TDCs is 2.5 ns (which is itself considerably better than required, since each track will have numerous timing measurements) we have conservatively limited the design length of each LVDS chain to 12 boards, which represents a factor of two safety margin ($12 \times 100\,\mathrm{ps} = 1.2\,\mathrm{ns}$) from a single TDC count. As LVDS is a mature technology, used in many consumer applications, this risk is a relatively mild one, which in the worst case would require fabrication of a small number of additional VME readout boards and/or a modest compromise in timing resolution which will not noticeably degrade the experiment's physics capabilities. Based on results from the first prototype, the final version of the LVDS interface will be designed and incorporated into the second (64-channel) prototype, and the full token-ring communication protocol defined, for testing together with a prototype of the VME readout controller.

2.6 FPGA and firmware

The internal behavior of the front-end board is supervised by an FPGA operating as a finite-state machine, making the system programmable and highly flexible. As noted, during commissioning of the first prototype version of the board during 2004 R&D, the most mission-critical and timing-sensitive elements of the firmware (controlling the TriP-t chip's buffering and TDC functionality) have already been developed and successfully tested. For the production boards, logic to interpret commands and exchange data over the LVDS interface, and control the Cockroft-Walton high-voltage supply will also be required. This additional logic can be developed and tested using the full 64-channel prototype version to be built in the summer 2006.

[1] For testing and commissioning the board's core digitization functionality, an alternative parallel-port interface was used during initial R&D studies.

Item	Cost $
Tooling costs	20
PC Board	100
Board assembly	200
Parts, components, & connectors	227
TOTAL	**547**

Table 3: Cost breakdown (per board) for MINERνA front-end boards(FEB).

Component	Cost $
ADCs	51
FPGA	26
Connectors	36
Regulators	46
Other	68
Subtotal	227

Table 4: Component cost breakdown (per board) for MINERνA front-end boards.

Persistent storage for the firmware is provided by an onboard flash PROM, which is read by the FPGA on power-up and can be re-written under computer control. As such, it will be possible to reprogram the FPGA logic of all boards remotely even after they are installed, if necessary.

2.7 Physical Components and Costs

The main costs and a breakdown of the components of the front-end electronics are shown in Tables 3, 4, 5, 6, and 7 for the Front-End Boards, Front-End Support Boards, Transition Boards, and PMT Crockroft-Walton base respectively. These costs are based on current price quotes and actual costs for the purchase of similar components for the initial front-end prototype fabrication. The cost of each item includes a 20% contingency which is estimated based on currently available prices (these estimates do not assume any quantity discounts).

3 Data acquisition and slow control

MINERνA's data acquisition (DAQ) requirements are relatively modest, as the average data rate expected in the NuMI beam is only 100 kByte/second and a two-second window for readout is available after each $\sim$ 10 μs spill. Moreover, the predictable timing of the beam obviates the need for a complicated trigger -

Item	**Cost $**
Tooling costs	20
PC Board	20
Board assembly	40
Parts, components, & connectors	83
TOTAL	**163**

Table 5: Cost breakdown (per board) for MINERνA front-end support boards(FESB).

Item	**Cost $**
Tooling costs	20
PC Board	15
Board assembly	30
Parts, components, & connectors	59
TOTAL	**124**

Table 6: Cost breakdown (per board) for MINERνA PMT Transition boards.

Item	**Cost $**
Tooling costs	20
PC Board	15
Board assembly	30
Parts, components, & connectors	30
TOTAL	**95**

Table 7: Cost breakdown (per board) for MINERνA Crockroft-Walton PMT Base.

instead, a gate is opened just prior to arrival of the beam, and all charge and timing information from the entire detector is simply read-out after the spill is complete. The slow-control system is also relatively simple, with each PMT powered by its own local Cockroft-Walton HV supply.

The DAQ and slow-control system is therefore essentially a communication network for distributing information (synchronization, high-voltage commands, and exceptionally, updated firmware) to the front-end boards and funnelling event data collected from them to the main data acquisition computer. The system consists of the following components:

- The main DAQ computer, including a VME interface board,
- Two VME crates containing a total of 10 custom-built Chain Read-Out Controller (CROC) modules, with each CROC controlling four LVDS chains,
- 42 LVDS chains (CAT-5e network cable), with each chain linking 12 front-end boards, and
- A third VME crate, containing timing, diagnostic and logic modules.

Due to the distributed nature of the front-end digitizer/high-voltage boards, the central DAQ and slow-control system itself can be easily accommodated in a single electronics rack.

3.1 LVDS token-ring chains

As explained in Section 2.5, the front-end digitizer boards are daisy-chained into 40 LVDS token rings of 12 boards each. Both ends of a chain terminate in a custom built VME chain read out controller (CROC) module described below. The number of digitizers on a chain is limited by the allowable jitter in the high-precision timing information transmitted to each digitizer board over LVDS. As LVDS is a one-way protocol, each digitizer board must receive the period global synchronization signal from the previous member of the chain on one connection, and re-transmit it to the next member on a second connection. From tests using our prototype boards we estimate that each board in a chain will introduce approximately 100 ps of jitter; thus a chain consisting of 12 boards would translate into roughly 1.25 ns timing jitter (worst case). This represents a factor of two saftey margin over the 2.5 ns least-count timing resolution of the front-end TDC's. In the unlikely event the jitter introduced by a chain of 12 front-end boards proves unacceptable, even with this large safety factor, the number CROC modules (and hence chains) could be increased, allowing each chain to have fewer members.

LVDS signals will be transmitted around a ring on standard, commercially-available fire-resistant and halogen-free CAT-5e network cable approved by Fer-

Figure 3: Photo of Prototype CROC 6U VME module.

Item	**Cost $**
Tooling costs	20
PC Board	330
Board assembly	240
Parts, components, & connectors	602
TOTAL	**1192**

Table 8: Cost breakdown (per board) for MINERνA Prototype Chain Read-Out Controller(CROC).

milab safety division for underground use. The LVDS chains will also be used to transmit configuration and slow-control messages to the cards.

3.2 Chain read-out controller (CROC) modules

Each CROC module(see figure 3 and table 8 will control four LVDS chains, requiring a total of 10 CROCs (plus spares) for the entire detector. These modules will reside in two VME crates alongside a crate controller and a MINOS timing distribution module.

The readout controller modules have the following functions:

1. Prior to the arrival of a NuMI spill, as signaled by the VME-resident MINOS

timing module, to reset the timing counters of each front-end board and open a 10μsec gate to collect data from the spill.

2. Upon completion of a NuMI spill, to initiate readout of front-end digitizer data over the four associated LVDS rings, into internal RAM.

3. Upon completion of the parallel readout of all four chains, to raise an interrupt with the main DAQ computer, indicating that event data is available. The PVIC/VME interface/crate controller allows VME interrupts to be received directly by the main computer.

4. The internal RAM of each CROC is memory-mapped to the host computer's PCI bus, allowing block transfer of event data via the PVIC/VME interface/crate controller. The relatively long NuMI duty cycle ($\sim$2 seconds) and low data rate (under 1MB per spill for the entire detector) ensures that no deadtime will be associated with the readout itself.

5. Once per second, to globally synchronize the detector's TDCs over LVDS using a high-precision refresh signal from the MINOS timing module. The need for this synchronization drives the choice of LVDS for the readout chains, as opposed a less performant alternative such as Ethernet.

6. Upon command of the main data acquisition computer, to control and monitor the Cockroft-Walton high-voltage power-supplies and to configure the firmware of these boards at run-startup.

3.3 VME backbone

Communication between the main data acquisition computer will be via commercially avaialble PVIC/VME link, allowing block data transfers to and from VME and interrupts to be received by the computer in response to the NuMI spill gate.

3.4 Ancilliary electronics

A trigger scaler and TDC to monitor the NuMI timing signals, and a programmable pulse generator to simulate them during beam-off periods, along with other any additional logic needed for monitoring and calibration, will reside in the third VME crate. All VME components will be installed underground, within about 20 meters of the detector.

3.5 Data acquisition computer

The main DAQ and slow-control computer will be located near the VME electronics, in the NuMI hall, with two high-speed TCP/IP links (one for data, one for

monitoring and control messages) to the Fermilab network. A relatively modest, dual-CPU server model will be more than adequate for our purposes. One CPU will be dedicated to real-time data acquisition, and the other will handle control messages and monitoring. An on-board, RAID-5 disk cluster with sufficient capacity to store several weeks of data will serve as a buffer for the data, pending transfer to offline processing nodes and permanent storage.

4 Interface to other Systems and Schedule

The following electonics will be provided to the following systems:

- PMT Boxes: All(473) Transition boards/cables (Interface between PMT base and FEB)
- PMT Testing: All(473) PMT bases, 7 FEB/FESB, 1 CROC, and stand-alone DAQ system for PMT testing
- Module Assembly/Mapping: 7 PMT bases, 7 FEB/FESB, 1 CROC, and stand-alone DAQ system for module scanning

For Fall 2006 the required electronics for both PMT Testing and Module remapping will be delivered. The components are enumerated above. During Spring 2008 the tracking prototype should come online and will require:

- 100 FEB/FESBs and 3 CROCs
- Prototype DAQ which includes VME Crate, PC card, and PC Readout software
- 100 PMT Boxes: Therefore 100 CW Bases/100 transition boards, plus cables to assemble the boxes

Component	Number	Comments
Channels	30272	WLS Fibers
Front-end boards	473	One per PMT, plus 15% spare
Readout Token Rings	40	12 PMTs/ring
VME Readout Cards	10	4 rings/card, plus five spare
VME Crates	3	Plus one spare
VME PVIC Interface	3	One per crate, plus one spare
PVIC/PCI Interface	1	Plus one spare
DAQ Computer with RAID system	1	Data rate is 120 kByte/spill

Table 9: Parts count for MINERνA electronics design

- LV Distribution

For the full detector:

- FEB Boards: 473 (545 w/spares)
- CROC Boards: 10 (14 w/spares)
- PMT bases: 473 (545 w/spares)
- Final DAQ system: VME Crate, PC card, and PC Readout software

The design of the readout electronics will be done at FNAL while the DAQ at the University of California, Irvine and FNAL. The production of the electronics will be outsourced while the testing, Q/A and installation will the responsibility of University of Pittsburgh and Northwestern University. DAQ production and installtion is the responsibility UC Irvine.

References

[1] "MCM II and the Trip Chip", J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, August 2002, FERMILAB-TM-2226.